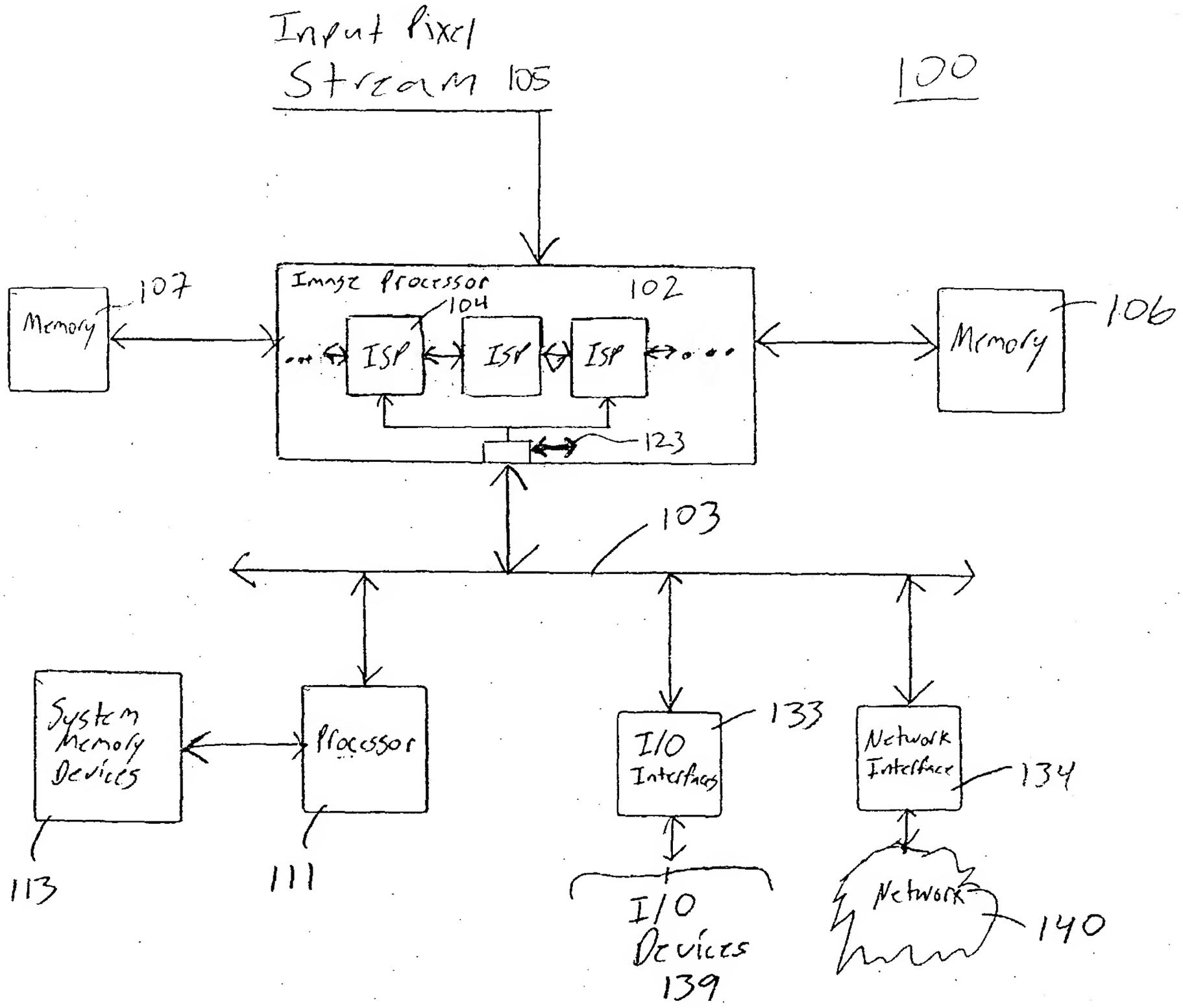
Input Pixel Stream 105
100
Memory
107
Image Processor
102
104
ISP
ISP
ISP
123
Memory
106
103
System Memory Devices
113
Processor
111
I/O Interfaces
133
I/O Devices 139
Network Interface
134
Network
140

Figure 1

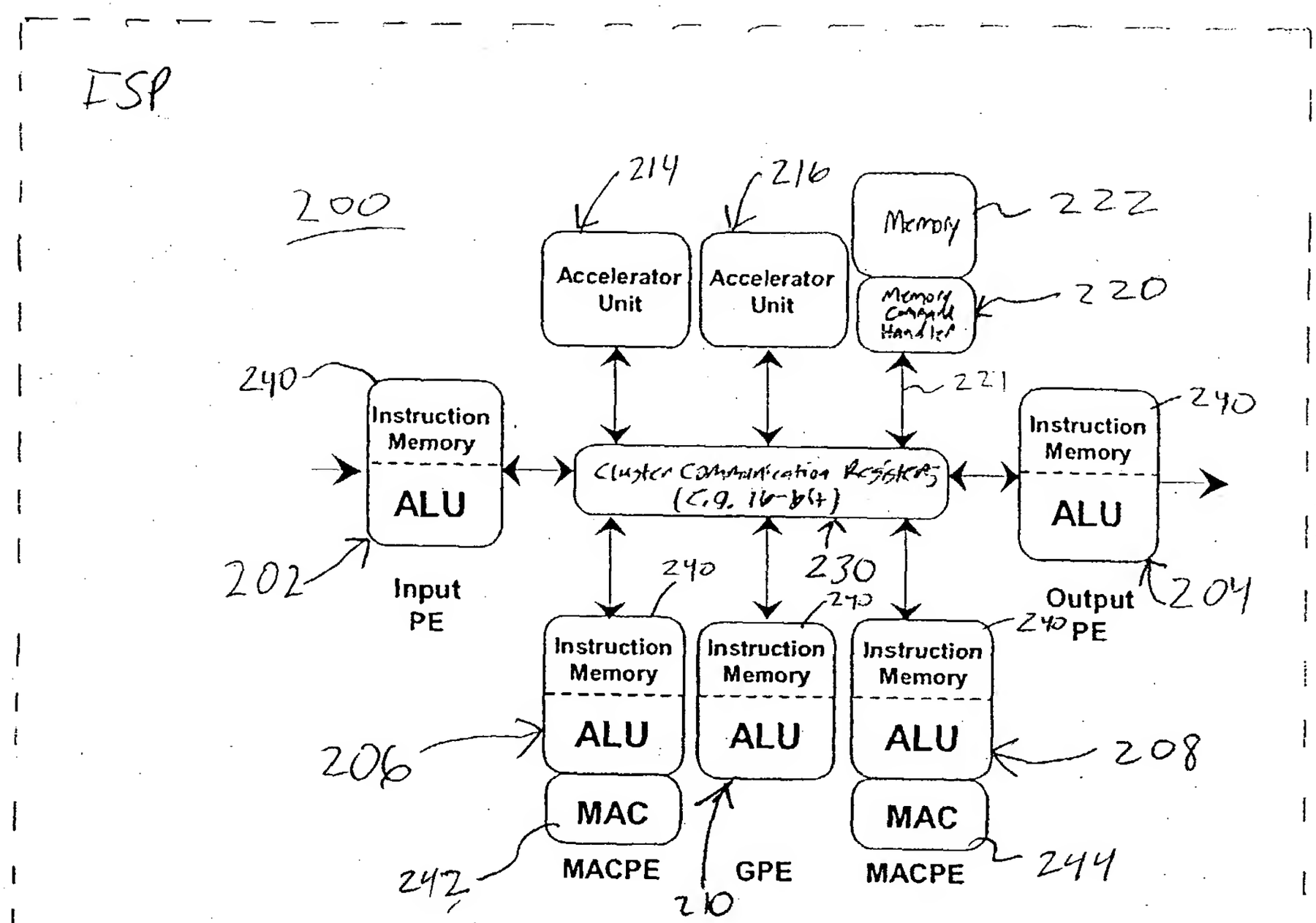
FSP
200
214
216
Memory
222
Accelerator Unit
Accelerator Unit
Memory Command Handler
220
240
Instruction Memory
ALU
221
Cluster Communication Registers (e.g. 16-bit)
240
Instruction Memory
ALU
202
Input PE
230
240
240
240
Output PE
204
Instruction Memory
ALU
MAC
Instruction Memory
ALU
Instruction Memory
ALU
206
208
MAC
MAC
242
MACPE
GPE
MACPE
244
210

Figure 2

300

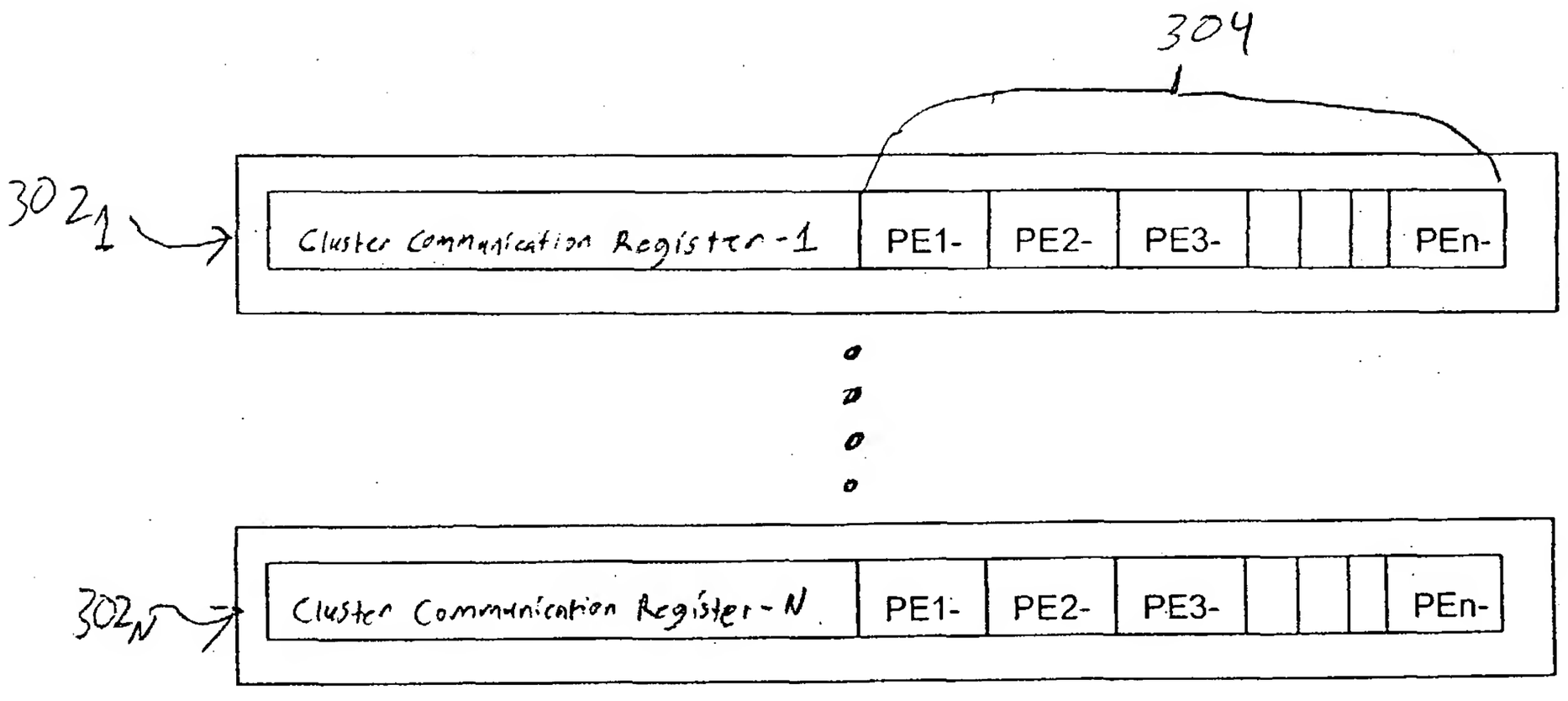
304
302 1
Cluster Communication Register-1
PE1-
PE2-
PE3-
PEn-
302 N
Cluster Communication Register-N
PE1-
PE2-
PE3-
PEn-

Figure 3

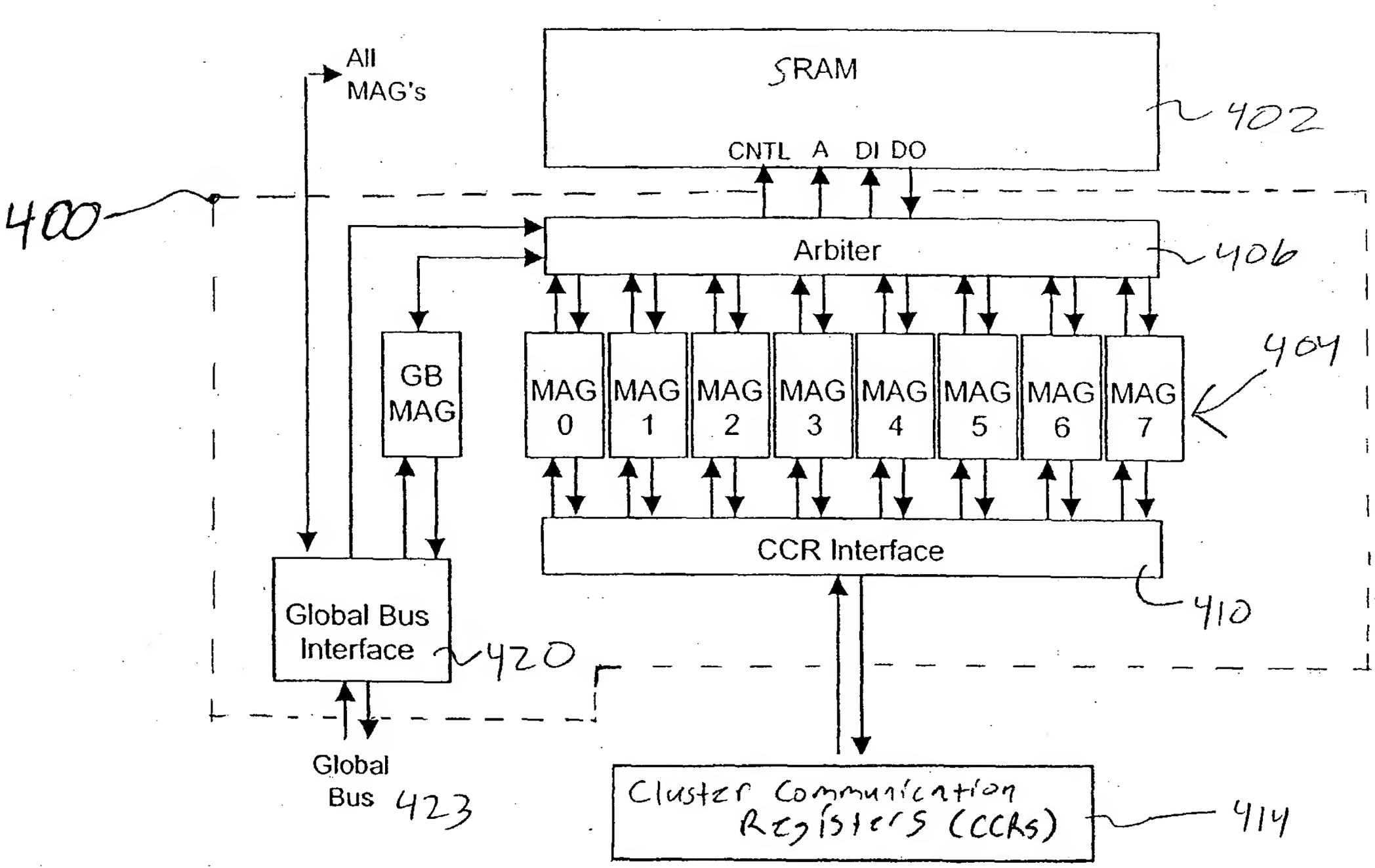
All MAG's
SRAM
402
CNTL A DI DO
400
Arbiter
406
GB MAG
MAG 0
MAG 1
MAG 2
MAG 3
MAG 4
MAG 5
MAG 6
MAG 7
404
CCR Interface
410
Global Bus Interface
420
Global Bus
423
Cluster Communication Registers (CCRs)
414

Figure 4

500

MAG	MAG0	MAG1	MAG2	MAG3	MAG4	MAG5	MAG6	MAG7
CCR0	Command							
CCR1	Data							
CCR2		Command						
CCR3		Data						
CCR4			Command					
CCR5			Data					
CCR6				Command				
CCR7				Data				
CCR8					Command			
CCR9					Data			
CCR10						Command		
CCR11						Data		
CCR12							Command	
CCR13							Data	
CCR14								Command
CCR15								Data

502
504
506
508
510
512

Figure 5

600

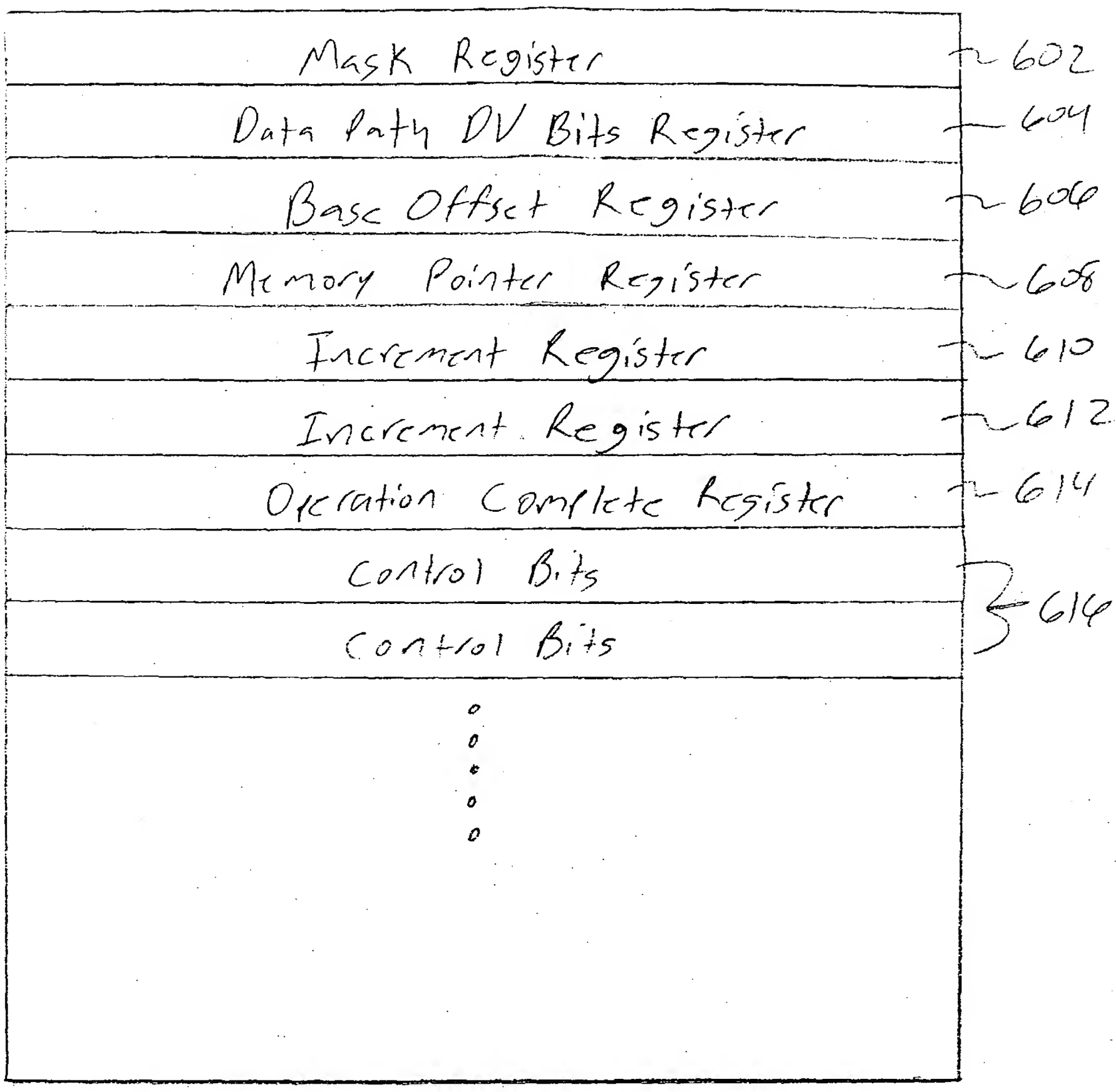
MAG
Mask Register
602
Data Path DV Bits Register
604
Base Offset Register
606
Memory Pointer Register
608
Increment Register
610
Increment Register
612
Operation Complete Register
614
Control Bits
Control Bits
616

Figure 6

700

	MCH Command	Description
702	Write Mask	Used in address calculations to create circular buffer addressing
704	Set Data Path DV bits	Determines the target PE(s) for the read data
706	Read Immediate	Reads RAM from a specified address
708	Write Immediate	Writes RAM from the Data CCR to a specified RAM address
710	Write MPR	An initial offset value to be used in address calculations
712	Write Increment Register	Provides X and Y increment values for one or 2D addressing
714	Write Base Offset Register	Sets the Base Offset Register used in addressing
716	Read Indirect, N Words	Reads N words into the Data CCR using the MAG Memory Pointer
718	Write Indirect, N Words	Writes N words from the Data CCR using the MAG Memory Pointer
720	Read Op Complete	Used to signal the MCH control PE that a block transfer is complete
722	Infinite Indirect Operation	Set infinite indirect MCH operation

Figure 7

800

802

15	14	13	12	11	10	9	8-0	
0	0	x	x	x	x	x	x	Read Immediate
1	0	x	x	x	x	x	x	Write Immediate
0	1	0	x	x	x	x	x	Read Indirect
0	1	1	x	x	x	x	x	Write Indirect
1	1	0	1	x	x	x	x	Write Increment Registers
1	1	0	0	0	x	x	x	Set Data Path
1	1	0	0	1	0	0	x	Set Read Operation Complete
1	1	1	0	0	x	x	x	Write Memory Pointer Register
1	1	1	0	1	x	x	x	Write Base Offset
1	1	1	1	0	x	x	x	Write Mask Register
1	1	1	1	1	x	x	x	Write First Use Registers

Figure 8